

Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims

Claims 1-19 (canceled)

Claim 20 (new): A modulator comprising:

a PLL circuit which detects a phase difference between an input signal of which a frequency is divided and a reference signal;

an AGC circuit which controls a gain of a modulating signal based on the input signal of which a frequency is divided, and which outputs a control signal; and

a voltage controlled oscillation circuit which controls an oscillation frequency of a signal outputted from said PLL circuit based on said control signal, wherein said voltage controlled oscillation circuit includes;

a first voltage controlled reactance unit which inputs said signal outputted from said PLL circuit;

a second voltage controlled reactance unit which inputs said control signal; and

a high-frequency oscillation circuit connected in parallel with said first and second voltage controlled reactance units, which outputs said input.

Claim 21 (new): The modulator according to claim 20, wherein the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, wherein the cathodes of the first and second varactor diodes are connected to each other, and wherein the signal outputted from the PLL circuit is inputted where the cathodes are connected to each other.

Claim 22 (new): The modulator according to claim 21, wherein the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, wherein the cathodes of the third varactor diode and fourth varactor diode are connected to each other, and wherein the control signal is inputted where the cathodes are connected to each other.

Claim 23 (new): The modulator according to claim 20, wherein the PLL circuit comprises:

- an oscillator which generates the reference signal;
- a frequency divider which divides a frequency of the input signal; and
- a comparator which compares the reference signal and the divided input signal to detect the phase difference.

Claim 24 (new): The modulator according to claim 20, wherein the first voltage controlled reactance unit includes a first varactor diode and a first capacitor, wherein a cathode of the first varactor diode is connected to one end of the first capacitor, and wherein the signal outputted from the PLL circuit is inputted where the cathode and the one end are connected to each other.

Claim 25 (new): The modulator according to claim 24, wherein the second voltage controlled reactance unit includes a second varactor diode and a second

capacitor, wherein a cathode of the second varactor diode is connected to one end of the second capacitor, and wherein the control signal is inputted where the cathode and the one end are connected to each other.